Characterization of ESD-induced electromigration on CMOS metallization in on-chip ESD protection circuit

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Electrostatic discharge (ESD) and electromigration are critical issues that significantly impact the reliability of ICs. While both of these phenomena have been studied independently, the combination of the two, ESD-induced electromigration, has received less attention, potentially compromising IC reliability. This work analyzes various types of metal with different lengths, widths, and angles commonly used in ESD protection circuits in the CMOS process. The objective is to observe their behavior under continuous ESD zapping. The ESD-induced electromigration of metallization in the CMOS process has been analyzed, and metal sensitivity to system-level ESD events has also been identified. It is also analyzed from the perspective of energy that the ESD energy that metal can withstand will decrease as the ESD voltage increases, which will be even more detrimental to the ESD reliability of ICs. The findings from this study aim to provide valuable insights for designing metal lines in ICs to enhance ESD protection.

1. Introduction

The reliability of ICs has always been an essential issue for electronics. Electrostatic Discharge (ESD) can generate currents of several amperes instantaneously, leading to irreversible damage to ICs.1,2 Therefore, an appropriate on-chip ESD protection circuit is necessary for ICs. Figure 1 shows a typical architecture of a whole-chip ESD protection circuit.3–5 The power-rail ESD clamp circuit is used to discharge the ESD current from VDD to VSS,6–8 and the protection devices can help to deal with the ESD current from I/O Pad to the power rail to avoid excessive ESD current from entering the internal circuit and causing it to burn out.9–11 Due to the large ESD current, the thicker top metal in the CMOS process is used to connect the protection devices and the power rail. Hence, the ESD robustness of metal should also be taken seriously to prevent it from becoming a breach in ESD protection. Especially in recent years, with the rapid development of system on a chip, it is possible to integrate the entire system with only one chip.12–14 Therefore, manufacturers are gradually focusing on chip system-level ESD robustness and conducting relevant tests. The relevant verification standards can refer to IEC 61000-4-2 and ESDA ESD-SP5.6-2019, and the discharge waveform is shown in Fig. 2.15,16

In contrast to ESD, which instantaneously destroys circuits, the metal used to connect components during regular use is susceptible to a failure phenomenon known as Electromigration.17–19 For metal, the long-term flow of current is akin to many electrons constantly hitting metal particles. Over time, the metal particles may shift in the current direction, as shown in Fig. 3.20–22 If there is an imbalance between the input and output flux of particles, particularly at corners, it poses a threat to the reliability of the metal. As shown in Fig. 4, when the inflow of metal particles is less than the outflow, it is referred to as a “void,” which may cause an open circuit. On the other hand, when metal particles accumulate in certain regions, they form a protrusion known as a “hillock.” These hillocks can pose a risk of creating a short circuit.23–25

While ESD and electromigration have been extensively studied as separate phenomena, less attention has been given to the combination of the two, known as ESD-induced electromigration.26–28 However, with the rapid scaling of process technology, the thickness of the back end of line metallization is reduced, which in turn decreases its maximum current density and ESD robustness. Although the impact of multiple ESD events on metal has been roughly verified, limitations in simulation software make it challenging to accurately determine the ESD robustness of metal.29–31 Even most of the process factories only provide maximum current under DC conditions. As a result, the layout of ESD protection circuits has often relied on experience or information from previous literature. It is necessary to conduct comprehensive research on the ESD robustness of metal to avoid open circuits caused by the metal being damaged by ESD earlier than the protection devices due to accidental layout choices.

In this work, the impact of multiple system-level ESD on the top metal in a CMOS process of Al FSG with different lengths, widths, and angles is studied. The current-voltage curve is also continuously observed to confirm the impedance of metal and whether they are conductive. In this work, it was found that the top metal layer is highly sensitive to system-level ESD, and even a slight voltage change can seriously affect its robustness. Also, the ESD robustness of metal is tried to analyze and predict from the energy perspective, and it finds that metal can withstand will decrease with the increase of ESD voltage. The data obtained from this research can serve as a valuable reference for future designs of ESD protection circuits. Implementing the insights gained from this study can enhance the overall ESD robustness of the chips.

2. ESD robustness verification methods

2.1 Testkeys design

To verify the impact of metal length and width on metal ESD robustness, this work used the top metal in the CMOS process, which is aluminum (Al) with a thickness of 2.34 μm. The length design is based on the minimum design rule of a
width of 1.5 μm and extended to 3, 6, and 12 μm; at the same time, the length part has 25, 50, 100, and 200 μm. Also, to know whether the metal corner angle will reduce its ESD robustness, this work designed different angles of the testkeys for each width (with a consistent length of 100 μm), with 90° and 135°, like Fig. 5. "Angle" is the interior angle between the metal on both sides and "Length" is the length of the centerline of the metal. The whole chip layout and the actual chip photo are shown in Figs. 6 and 7. The chip is also bonded for the convenience of subsequent measurements, as shown in Fig. 8. The wire diameter of the gold wire used is ensured to be much larger than that of the metal to be tested to avoid affecting the experimental results.

2.2. Measurement methods

The ESD Gun, like Fig. 9, is used to generate the system-level ESD with the IEC 61000-4-2 standard in this work. The measurement methods are as follows: First, the semiconductor characterization system was used to measure the initial current-voltage curve (I-V curve) of the testkeys before being zapped by ESD as a follow-up reference. Then, selecting the ESD voltage to be tested, use the ESD Gun to zap a fixed number of contact-mode discharges per round. After each round of zapping, measure the I-V curve again, and judge whether the testkeys are damaged by the open circuit according to the current value. Repeat the above steps and apply ESD if no obvious abnormality is found. On the contrary, if the open circuit is evident or the accumulative zap times are more significant than 1000 times, record the failure voltage and accumulative zap times.

3. Verification results of straight metal

3.1. Changes in The I-V curve of metal before and after ESD

The measurement results are shown in Table I, and the photos of the testkeys before and after ESD are shown in Fig. 10. It can be seen that there is an apparent failure on the metal line. Here, as an example, take the testkeys L25_W6 and L200_W6 with the same width but three times the difference in length. After repeated zapping by 5.4 kV and 5.45 kV system-level ESD, the I-V curves of the two are drawn, respectively, as shown in Figs. 11 and 12 (the number of times in the figure is the accumulative zap times).

It is known that the increase in metal length will increase the probability of electromigration and reduce the lifetime of metal. Also, the impedance of metal will gradually increase with the test time extending and eventually opening the circuit. However, these phenomena were not found in this work. There is no significant difference in the ESD robustness between the threefold difference in the metal length. At the same time, no matter what the failure voltage is, it is not found that the I-V curve gradually shifts during the test but tends to open instantly. It means that regardless of the applied ESD voltage and the length of the metal, it will fail immediately after the zap times it withstands reach the upper limit.

It may be speculated that compared with the traditional electromigration test current since the ESD current is large enough, many electrons can push the metal particles...
simultaneously instead of moving them gradually. At the same time, unlike the stable temperature experimental environment of electromigration, the temperature gradient rise caused by the instantaneous large current of ESD also accelerates the failure of the metal. Hence, there is no drift in the measured impedance of metal here, meaning that metal is far more susceptible to ESD than expected. ESD-induced electromigration may destroy the metal at any time and render the ESD protection circuit ineffective, making predicting ESD robustness more difficult.

3.2. The influence of length and width on straight metal ESD robustness

To confirm whether the length and width of the metal will affect its ESD robustness, the measurement results are plotted as a line graph, as shown in Fig. 13. Similar to the previous results, the failure voltage is roughly proportional to its width. However, its relationship with its length is not apparent. It can be inferred that because ESD is an instantaneous high-current event, compared with the traditional electromigration measurement current, the metal width directly affecting the current density will be more dominant than the length. So, if the metal current density is approximately the same, it is reasonable that the failure voltage is proportional to its width.

On the other hand, ideally, the accumulated zap times that a metal can withstand under different failure voltages should decrease slowly as the voltage rises. However, the data here shows that only a tiny failure voltage change may lead to an avalanche drop in metal robustness. Taking the testkey L200_W6 as an example, the failure voltage is only increased from 5.4 kV to 5.43 kV, and the zap times it can withstand drops from more than 1000 to 85 times. It can be speculated that the metallization layer may be much more sensitive to ESD than expected. This will not be conducive to the design of ESD protection circuits and may also reduce the long-term use lifetimes of metal damaged by ESD.

3.3. Discussion

Ideally, the total ESD energy that can withstand per unit width of the metal should be close to each other. In other words, even if a different voltage of ESD is applied to the same width of the metal, the energy value of each ESD multiplied by the zap times should be the same. However, it can be seen from the previous results that only a tiny change in failure voltage will
Table I. The measurement results of the testkeys with different lengths and widths.

<table>
<thead>
<tr>
<th>Cell name</th>
<th>Length ((\mu)m)</th>
<th>Width ((\mu)m)</th>
<th>Failure voltage and zap times</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Device 1</td>
</tr>
<tr>
<td>L25_W1.5</td>
<td>25</td>
<td>1.5</td>
<td>1.63 kV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&gt;1000 times</td>
</tr>
<tr>
<td>L25_W3</td>
<td>25</td>
<td>3</td>
<td>2.9 kV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>800 times</td>
</tr>
<tr>
<td>L25_W6</td>
<td>25</td>
<td>6</td>
<td>5.4 kV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>440 times</td>
</tr>
<tr>
<td>L25_W12</td>
<td>25</td>
<td>12</td>
<td>10.3 kV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>390 times</td>
</tr>
<tr>
<td>L50_W1.5</td>
<td>50</td>
<td>1.5</td>
<td>1.65 kV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&gt;1000 times</td>
</tr>
<tr>
<td>L50_W3</td>
<td>50</td>
<td>3</td>
<td>2.9 kV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&gt;1000 times</td>
</tr>
<tr>
<td>L50_W6</td>
<td>50</td>
<td>6</td>
<td>5.38 kV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100 times</td>
</tr>
<tr>
<td>L50_W12</td>
<td>50</td>
<td>12</td>
<td>10.3 kV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400 times</td>
</tr>
<tr>
<td>L100_W1.5</td>
<td>100</td>
<td>1.5</td>
<td>1.63 kV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&gt;1000 times</td>
</tr>
<tr>
<td>L100_W3</td>
<td>100</td>
<td>3</td>
<td>2.88 kV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&gt;1000 times</td>
</tr>
<tr>
<td>L100_W6</td>
<td>100</td>
<td>6</td>
<td>5.3 kV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&gt;1000 times</td>
</tr>
<tr>
<td>L100_W12</td>
<td>100</td>
<td>12</td>
<td>10.5 kV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>980 times</td>
</tr>
<tr>
<td>L200_W1.5</td>
<td>200</td>
<td>1.5</td>
<td>1.65 kV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&gt;1000 times</td>
</tr>
<tr>
<td>L200_W3</td>
<td>200</td>
<td>3</td>
<td>2.9 kV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&gt;1000 times</td>
</tr>
<tr>
<td>L200_W6</td>
<td>200</td>
<td>6</td>
<td>5.4 kV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&gt;1000 times</td>
</tr>
<tr>
<td>L200_W12</td>
<td>200</td>
<td>12</td>
<td>10.5 kV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&gt;1000 times</td>
</tr>
</tbody>
</table>

Fig. 10. The photos of the testkey L50_W12 (a) before ESD and (b) after 10.4 kV ESD. It can be seen that the metal, after ESD zapping, shows noticeable burn marks.

Fig. 11. I-V curve measurements of L25_W6 under (a) 5.4 kV and (b) 5.45 kV ESD test (current limited to 100 mA).
cause the ESD robustness of the metal to drop avalanche. Therefore, it is reasonable to speculate that the ESD energy that metal can withstand may decrease as the voltage increases. This work explores the phenomenon and draws conclusions.

Equation (1) for calculating the Withstand Energy Change Rate (WECR) is used to analyze the change of ESD energy per unit width metal can withstand. In this equation, $P_{total}$ represents the accumulated ESD energy applied to the metal under this failure voltage measurement. It is obtained by multiplying the zap times by the energy of a single ESD discharge, which is the product of the ESD failure voltage ($V_{ESD}$) and the peak ESD current ($I_{ESD}$). For the system-level ESD used in this work, the peak current of each 1 kV of ESD is about 3.65 A, which means the energy is approximately 3.65 kJ. Then, through the failure voltage difference and metal width to normalize, the decrease in ESD energy per unit width metal can withstand every time the applied voltage increases by 1 volt can be calculated.

$$WECR = \frac{\Delta P_{total}}{\Delta V_{ESD} \times \text{Width}}$$

To explore the condition where the ESD robustness of metal decreases the most, the part with the most significant slope of each testkey in Figs. 13(a) and 13(b) is used to calculate $WECR$. The results are shown in Table II and plotted in Fig. 14. It can be seen that when the length of the
metal is longer, the ESD energy it can withstand decreases more as the voltage increases. Combined with the observations above, it can be inferred that although the length of the metal does not affect the failure voltage range, it does affect its sensitivity to ESD. The longer the metal, the more sensitive to ESD.

Therefore, the results here can provide suggestions for layout designers of ESD protection circuits: Compared with the length, the metal width will directly affect the failure voltage range of the metal, so the layout should consider the width of the metallization as comprehensively as possible. But this does not mean that length is not necessary. More extended metals may affect the average use lifetime of the overall circuit. They will also make it more sensitive to ESD, increasing the uncertainty in evaluating the robustness of the overall circuit. At the same time, the measurement results here can also be used to assess the ESD robustness of the overall circuit to avoid the metal used to connect the protection devices burning earlier.

4. The influence of angle on metal ESD robustness

4.1. Measurement results

Since only having straight metal in the circuit layout is impossible, this work also designed 90° and 135° corners for metals of different widths. It investigated the corner of the metal on its ESD robustness. Figure 15 is the photo of the testkey A135_W12 before and after ESD, and an apparent burnt condition at the corner can be seen, which proves that this is the most vulnerable place. The list of testkeys and their system-level ESD measurement results are shown in Table III, and the results are also plotted in Fig. 16.

<table>
<thead>
<tr>
<th>Cell name</th>
<th>Angle</th>
<th>Width (μm)</th>
<th>Length (μm)</th>
<th>Failure voltage and zap times</th>
</tr>
</thead>
<tbody>
<tr>
<td>L100_W1.5</td>
<td>180°</td>
<td>1.5</td>
<td>100</td>
<td>Device 1  Device 2  Device 3</td>
</tr>
<tr>
<td>A135_W1.5</td>
<td>135°</td>
<td>1.5</td>
<td>100</td>
<td>1.6 kV &gt;1000 times 1.63 kV &gt;1000 times 1.65 kV 120 times</td>
</tr>
<tr>
<td>A90_W1.5</td>
<td>90°</td>
<td>1.5</td>
<td>100</td>
<td>1.6 kV &gt;1000 times 1.63 kV &gt;1000 times 1.65 kV 15 times</td>
</tr>
<tr>
<td>L100_W3</td>
<td>180°</td>
<td>3</td>
<td>100</td>
<td>2.8 kV &gt;1000 times 2.83 kV &gt;1000 times 2.85 kV 5 times</td>
</tr>
<tr>
<td>A135_W3</td>
<td>135°</td>
<td>3</td>
<td>100</td>
<td>2.8 kV &gt;1000 times 2.83 kV &gt;1000 times 2.85 kV 5 times</td>
</tr>
<tr>
<td>A90_W3</td>
<td>90°</td>
<td>3</td>
<td>100</td>
<td>2.8 kV &gt;1000 times 2.83 kV &gt;1000 times 2.85 kV 5 times</td>
</tr>
<tr>
<td>L100_W6</td>
<td>180°</td>
<td>6</td>
<td>100</td>
<td>5 kV &gt;1000 times 5.2 kV &gt;1000 times 5.3 kV 5 times</td>
</tr>
<tr>
<td>A135_W6</td>
<td>135°</td>
<td>6</td>
<td>100</td>
<td>5 kV &gt;1000 times 5.2 kV &gt;1000 times 5.3 kV 10 times</td>
</tr>
<tr>
<td>A90_W6</td>
<td>90°</td>
<td>6</td>
<td>100</td>
<td>5 kV &gt;1000 times 5.2 kV &gt;1000 times 5.3 kV 5 times</td>
</tr>
<tr>
<td>L100_W12</td>
<td>180°</td>
<td>12</td>
<td>100</td>
<td>9.75 kV &gt;1000 times 10 kV &gt;1000 times 10.3 kV 5 times</td>
</tr>
<tr>
<td>A135_W12</td>
<td>135°</td>
<td>12</td>
<td>100</td>
<td>9.5 kV &gt;1000 times 9.75 kV &gt;1000 times 10 kV 5 times</td>
</tr>
<tr>
<td>A90_W12</td>
<td>90°</td>
<td>12</td>
<td>100</td>
<td>9.5 kV &gt;1000 times 9.75 kV &gt;1000 times 10 kV 25 times</td>
</tr>
</tbody>
</table>

Fig. 15. The photos of the testkey A135_W12 (a) before ESD and (b) after 9.75 kV ESD. It can be clearly seen that the failure location is at the corner of the testkey.
times. This will predictably increase the difficulty in predicting the ESD robustness of metal, meaning there are more factors to consider, which will be analyzed in the next.

4.2. Discussion

To more clearly see the damage of the corners to the ESD robustness of the metal, Fig. 17 plots the zap times of metals at different angles under a fixed failure voltage, which is selected roughly proportional to the width of the metal. It can be found that when the length and width are the same, the corner will significantly reduce the robustness of the metal to ESD, and there is a tendency to get worse as the angle decreases. It is also found that as the width of the metal increases, the robustness decreases more obviously. Although the selected ESD voltage is roughly proportional to the metal width, taking the width of 6 μm and 12 μm as an example, the zap times the metal with a 135° angle can withstand is much lower than that of a straight metal with a 180° angle, which is almost unable to resist any ESD zapping.

At the same time, in order to observe whether the corners of the metal will affect its sensitivity to ESD, Eq. (1) is also used here to evaluate the WECR value of the angled metal. The results are shown in Table IV and plotted in Fig. 18. Among them, the straight metals (L100_W1.5, L100_W3, L100_W6, and L100_W12) follow the data in Table II, while the metal with 135° and 90° in each width is obtained using the part with the largest slope in Fig. 16. Based on the above results, it can be found that although the corners of the metal will greatly reduce its robustness to ESD, it will make the metal less sensitive to ESD. It is speculated that due to the physical limitations at metal corners, the flux of metal particles there will be unequal, exacerbating the possibility of electromigration and reducing its robustness to ESD. At the same time, compared to straight metal, which may be burned along the metal, the failure points of bending angles are mostly concentrated at the corners, so the overall measurement results can be more consistent, making its sensitivity to ESD less obvious than that of straight metal. But in conclusion, it is still not recommended to lay out the metal with angles. The large area non-turning metal layout method will be more beneficial, and the research data in this work will help predict the circuit’s ESD robustness.

5. Conclusion

The impact of electromigration induced by the system-level ESD has been studied in the CMOS process. The results show that the range of failure voltage is roughly proportional to the width of the metal. Moreover, it has also been found that the longer the metals exhibit the higher sensitivity to ESD. Even slight variations in ESD voltage can lead to
significantly different results, which makes predicting and simulating the ESD robustness of metals difficult. At the same time, from the energy perspective, it can be found that the ESD energy that metal can withstand will decrease as the electrostatic voltage increases. On the other hand, the ESD robustness of metals with corners will be significantly reduced and may vary depending on the angle. The findings presented in this paper provide valuable insights for enhancing on-chip ESD robustness, which provides guidance for future metallization design and layout considerations aimed at improving on-chip ESD protection.

Acknowledgments

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