Impact of Inner Pickup on ESD Robustness of Multifinger MOSFET in 28-nm High-k/Metal Gate CMOS Process

Chun-Yu Lin, Member, IEEE, Pin-Hsin Chang, and Rong-Kun Chang

Abstract—The impact of pickup structure on electrostatic discharge (ESD) robustness of multifinger MOSFET in 28-nm high-k/metal gate CMOS process was investigated in this paper. Verified in silicon, the multifinger MOSFET without the pickup structure inserted into its source region can sustain the higher ESD level and more compact layout area.

Index Terms—Electrostatic discharge (ESD), layout, MOSFET, pickup.

I. INTRODUCTION

ALTHOUGH the high-k dielectric has been introduced in sub-50-nm CMOS technologies, the MOS transistors are still sensitive to electrostatic discharge (ESD), [1], [2]. Therefore, on-chip ESD protection circuits must be equipped for the pads that may be stressed by ESD. To achieve effective ESD protection, the voltage across the ESD protection circuit during ESD stresses should be carefully designed. First, the trigger voltage \( V_{t1} \) and holding voltage \( V_h \) of ESD protection circuit must be lower than the breakdown voltage of internal circuits to prevent from damage before the ESD protection circuit is turned on during ESD stresses. Second, the \( V_{t1} \) and \( V_h \) of the ESD protection circuit must be higher than the power-supply voltage of the IC to prevent the ESD protection circuits from being mis-triggered under normal circuit operating conditions. Moreover, the turn-on resistance \( R_{on} \) of ESD protection circuit should be minimized to reduce the joule heat generated in the ESD protection circuit and the clamping voltage of the ESD protection circuit during ESD stresses.

To discharge the high ESD energy without causing damage to internal circuits, the typical ESD protections include the gate-grounded NMOS (GGNMOS) and gate-VDD PMOS (GDPMOS) [3], [4]. When the GGNMOS or GDPMOS is under ESD stress, the parasitic NPN or PNP BJT will be triggered to discharge ESD current. To sustain the required ESD level, such a GGNMOS or GDPMOS is often designed with large dimension, which is often drawn with the multifinger style to reduce the total occupied layout area. However, it has been reported that multi-finger ESD protection devices in some CMOS processes can not be uniformly turned on under ESD stress [5]. That is, even if a larger multi-finger MOSFET is used as the ESD protection circuit, uniform conduction of all fingers is hard to achieve, and hence the expected ESD level can not be realized.

To solve this problem, several prior designs have been reported to enhance the turn-on uniformity [6]–[11]. Adding additional pickups into the layout of GGNMOS may be a solution [6], which makes the base resistance of each parasitic BJT approximately equal. With the equal base resistance, all parasitic BJT may be triggered on simultaneously to discharge ESD current. Besides, adding pickups makes the base resistance of each parasitic BJT smaller, which increases the collector-emitter voltage (holding voltage) during BJT on state, and then makes the GGNMOS less latch-up prone [12].

Since the average cost of a die in sub-50-nm technologies is much high, it is important to optimize ESD protection circuit to have a high ESD robustness within limited layout area. The effect of additional layout pickups to the ESD robustness of GGNMOS in submicron CMOS technologies have been reported [13], [14]. In this work, the effect of additional layout pickups to the ESD robustness of GGNMOS and GDPMOS in a 28-nm high-k/metal gate CMOS process is investigated. Although the foundry usually does not recommend adding the pickups into layout, the measurement results of this work can provide the reference silicon data for circuit designers to design their ESD protection in sub-50-nm technologies.

II. ESD PROTECTION MULTI-FINGER MOSFET WITH DIFFERENT NUMBER OF PICKUPS

The layout top view and the device cross-sectional view of an ESD protection multi-finger GGNMOS without additional pickup is shown in Fig. 1. In the multi-finger GGNMOS structure with \( P+ \)-guard ring surrounding it, the distances from the base regions of each parasitic NPN BJT to the \( P+ \) guard ring at top and bottom are the same; however, these distances at left and right are different. Although the distances from top and bottom to the base region are smaller than the distances from left and right, the \( P+ \) -guard ring still makes the base resistance of NPN BJT in the central region of the multi-finger GGNMOS higher than those in the side regions \( R_{well-3} > R_{well-2} > R_{well-1} \). Therefore, in the multi-finger GGNMOS structure, the center fingers are always triggered on faster than the others under ESD stress. The turn-on uniformity of the multi-finger GGNMOS should be investigated.

Fig. 2 shows the layout top view and the device cross-sectional view of an ESD protection multi-finger GGNMOS with an additional...
Fig. 2. Layout top view and device cross-sectional view of multi-finger GGNMOS with additional pickup.

Fig. 3. Layout top view of multi-finger GGNMOS with different number of pickups: (a) pickup = 0 (normal), (b) pickup = 1, (c) pickup = 2, and (d) pickup = 5.

Fig. 4. TLP I–V curves of test GGNMOS.

Fig. 5. TLP I–V curves of test GDPMOS.

$P^+$ pickup at source side. The additional $P^+$ pickup in GGNMOS is connected to the $P^+$ guard ring. With the additional $P^+$ pickup inserted into the GGNMOS, the base resistance ($R_{\text{well}}$) of each parasitic NPN BJT can be effectively balanced. From the viewpoint of $R_{\text{well}}$ symmetry of parasitic BJT, inserting additional $P^+$ pickups at source side of GGNMOS can improve turn-on uniformity during ESD stresses. However, it is known that the low $R_{\text{well}}$ of parasitic lateral BJT leads to the higher trigger current ($I_{\text{t1}}$) of GGNMOS. As a result, GGNMOS may be hard to turn on.

To clarify above-mentioned issues, the effect of additional layout pickups to ESD robustness of multi-finger GGNMOS in a 28-nm high-$k$/metal gate CMOS process is studied. The layout top views of GGNMOS with 0, 1, 2, and 5 $P^+$ pickups are shown in Fig. 3(a)–(d), respectively. The GGNMOS with 5 $P^+$ pickups indicates that this GGNMOS has pickup or guard ring beside each finger. All these test GGNMOS have the same effective device dimension of 240 $\mu$m and the same layout style, except for the $P^+$ pickups. Similarly, the GDPMOS with the same variables are tested.

### III. Experimental Results and Discussion

To investigate the turn-on behavior and the I–V curve in high-current region of the ESD protection circuit, the transmission-line-pulsing (TLP) system with 10-ns rise time and 100-ns pulse width is used. The TLP-measured I–V characteristics of the GGNMOS and GDPMOS are shown in Figs. 4 and 5, respectively. The trigger voltage ($V_{\text{t1}}$), the trigger current ($I_{\text{t1}}$), the holding voltage ($V_{\text{h}}$), the turn-on resistance ($R_{\text{on}}$), and the secondary breakdown current ($I_{\text{t2}}$) of the test devices are extracted and listed in Table I. It can be found that
TABLE I

DEVICE DIMENSIONS AND MEASUREMENT RESULTS

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<tbody>
<tr>
<td></td>
<td>W/L</td>
<td>Number of</td>
<td>HBM 1</td>
<td>HBM 2</td>
<td>TLP</td>
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<td>(μm/μm)</td>
<td>Pickups</td>
<td>Level 1 (V)</td>
<td>Level 2 (V)</td>
<td>V_t1 (V)</td>
</tr>
<tr>
<td>---</td>
<td>---</td>
<td>---</td>
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<td>---</td>
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</tr>
<tr>
<td>GGNMOS</td>
<td>240/0.13</td>
<td>0</td>
<td>1500</td>
<td>3000</td>
<td>4.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>1500</td>
<td>2750</td>
<td>4.5</td>
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<tr>
<td></td>
<td></td>
<td>2</td>
<td>1000</td>
<td>2500</td>
<td>4.7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5</td>
<td>275</td>
<td>2250</td>
<td>4.8</td>
</tr>
<tr>
<td>GDPRMOS</td>
<td></td>
<td>0</td>
<td>275</td>
<td>N/A</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>1</td>
<td>175</td>
<td>N/A</td>
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<td>125</td>
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<td></td>
<td>5</td>
<td>100</td>
<td>N/A</td>
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</table>

1 HBM ESD test from 0V.
2 HBM ESD test from 2000V.

the GGNMOS with more pickups have the poor performances (higher \( V_{t1} \), higher \( I_{t1} \), higher \( V_h \), higher \( R_{on} \), and lower \( I_{t2} \)) under TLP tests. The GDPRMOS have much lower \( I_{t2} \), and the pickups make it even worse. According to the experimental results, inserting additional pickups lowers the base resistance \( (R_{well}) \) of parasitic lateral BJT, and leads to the worse BJT performances.

The human-body-model (HBM) ESD robustness is tested. The failure criterion is defined as the I–V curve seen between test pads shifting over 30% from its original curve after ESD stressed at every ESD test level. All ESD robustness of the test devices are measured and listed in Table I. The GGNMOS with 0/1/2/5 \( P^+ \) pickups can pass at 3000 V/2750 V/2500 V/2250 V, but fail at 1500/1500/1000 V/275 V. It indicates that most of the fingers in GGNMOS can be turned on at higher stress voltage, but non-uniform conduction is observed at lower stress voltage. Each finger in the GGNMOS with \( P^+ \) pickups has lower ESD robustness due to its higher holding voltage. Besides, the fingers in the GGNMOS with \( P^+ \) pickups need higher voltage and current to trigger on, so the ESD robustness of GGNMOS with 2 and 5 \( P^+ \) pickups are seriously degraded at lower stress voltage. The similar results are found in the TLP tests.

The very fast TLP (VF-TLP) system with 0.2-ns rise time and 1-ns pulse width is used to capture the transient behavior of the test devices in the time domain of charged-device-model (CDM) ESD event. The VF-TLP-measured I–V curves of the GGNMOS and GDPRMOS are shown in Figs. 6 and 7, respectively. The trigger currents of the GGNMOS after adding \( P^+ \) pickups are not increased in such fast transient event, so all GGNMOS can achieve about 3.1 A VF-TLP-measured \( I_{t2} \). The parasitic PNP BJT in the GDPRMOS can also be triggered on in such fast transient event. The VF-TLP-measured \( I_{t2} \) of all GDPRMOS are about 2.4 A.

According to these measurement results, the inner pickup averaged the base resistance of each fingers, but it also suppressed the source-to-body potential (body effect) [15]. As a result, it made the GGNMOS hard to trigger during HBM and TLP tests, and the \( V_{t1} \) and \( I_{t1} \) became higher. Meanwhile, the \( V_b \) and \( R_{on} \) became higher, but the \( I_{t2} \) and ESD robustness became lower, which was due to the inner pickup inhibition of body effect. In short, inserting additional layout pickups into the multi-finger GGNMOS and GDPRMOS can increase the holding voltage, but it can not improve the turn-on uniformity. These experimental results provide the design guideline for ESD protection multi-finger MOSFET in 28-nm high-\( k \)/metal gate CMOS process.

IV. CONCLUSION

Effect of additional layout pickups to the ESD robustness of GGNMOS and GDPRMOS in the 28-nm high-\( k \)/metal gate CMOS process has been studied in this work. Experimental results show that inserting additional pickups has negative impact to the ESD protection level
of GGNMOS and GDPMOS. Besides, layout area of MOSFET expands due to the insertion of additional pickups. Therefore, additional pickups are not suggested for ESD protection multi-finger MOSFET in 28-nm high-k/metal gate CMOS process.

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REFERENCES